Claims

1. A phase-locked loop circuit comprising an oscillator (32) controlled in dependence on the output of a phase detector (30), an output amplifier (27) for amplifying the output of the oscillator (32) and a feedback path to the phase detector (30) from the output of the output amplifier (27), **characterised by** a second feedback path from the output of the oscillator (30) to the phase detector (30), by-passing the output amplifier (27), and control means (26, 40, 41) for disabling the output amplifier (27) when the loop circuit is not locked and interrupting the second feedback path when the loop circuit has become locked.

2. A circuit according to claim 1, wherein the second feedback path includes a variable gain amplifier (33), the control means (26, 40, 41) being configured to interrupt the second feedback path by reducing the gain of the variable gain amplifier (33).

3. A circuit according to claim 2, wherein the control means (26, 40, 41) is configured to interrupt the second feedback path by ramping down the gain of the variable gain amplifier (33).

4. A circuit according to claim 3, wherein the control means (26, 40, 41) is configured to ramp up the gain of output amplifier (27) on enabling thereof, the ramping down of the gain of the variable gain amplifier (33) overlapping the ramping up of the gain of output amplifier (27).

5. A circuit according to claim 4, including phase control means (37, 38, 39) for matching the phase of the output of the variable gain amplifier (33) to that of the output of the output amplifier (27) when both are operating.

6. A circuit according to claim 5, wherein the phase control means (37, 38, 39) comprises a variable delay (37) in the second feedback path, a phase detector (38) receiving a signal from the second feedback path downstream of the variable delay (37) and a signal from the first feedback path and a low-pass filter (39) for filtering

the output of the phase detector (38) to provide a delay control input signal for the variable delay (37).

7. A circuit according to any preceding claim, wherein the first and second feedback paths share a common portion.

8. A circuit according to claim 7, wherein the first and second feedback paths are united by a summer (34).

9. A circuit according to claim 7 or 8, wherein said common portion includes a frequency down converter (35, 36).

10. An envelope elimination and restoration transmitter including a circuit according to any preceding claim, wherein the first feedback path provides a feedback signal for a closed loop envelope restoration circuit, the control means (26, 40, 41) including an envelope controller (26) for controlling the gain of the output amplifier (27).

11. A mobile phone including a circuit according to any one of claims 1 to 9, wherein the output amplifier (37) is an RF power amplifier.